Synopsys to Distribute Tower Semiconductor's 0.18- and 0.13-Micron Silicon Libraries within DesignWare Library

Tower's Complete Set of Standard Cells, I/Os and Memory Compilers Available to More Than 25,000 DesignWare Library Users

MOUNTAIN VIEW, Calif. and MIGDAL HAEMEK, Israel — April 13, 2005 - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, and Tower Semiconductor Ltd. (NASDAQ: TSEM; TASE: TSEM), a pure-play independent specialty foundry, today announced that Tower's in-house set of 0.18-micron standard cells, I/Os and memory libraries are now available through Synopsys' DesignWare® Library. As a result, more than 25,000 DesignWare Library licensees now have access to Tower Semiconductor's 0.18-micron libraries, at no additional charge, for use in complex system-on-chip (SoC) designs. Starting in the third quarter of this year, licensees are expected to have access to Tower's 0.13-micron libraries.

The 0.18-micron libraries include a complete set of views fully validated in silicon in high-volume production, as well as views for third-party EDA tools. The library distribution agreement with Synopsys also includes the future distribution of Tower's 0.13-micron libraries through the DesignWare Library.

"We have successfully used the Tower 0.18-micron standard cells and I/Os in our design. The high quality of the library and the expert support staff from Synopsys enabled us to smoothly meet our design goals," said Alan Tsun, vice president of ESP development engineering at QuickLogic (NASDAQ: QUIK). "Including the Tower library in the DesignWare Library means our designers will have easy library access with effective support and regular updates. This greatly simplifies our IP procurement and administrative processes."

"Distributing our technology-optimized libraries through the Synopsys DesignWare Library enables us to reach out to a very large number of SoC designers who are targeting our 0.18-micron technologies," said Rafi Nave, vice president of customer services at Tower

Semiconductor. “We worked closely with Synopsys to ensure a smooth path to silicon and the support given by Synopsys’ experts will help ensure our customers’ design success.”

“With this library distribution agreement, Synopsys and Tower are answering designers’ requests for a complete RTL-to-GDSII design environment with streamlined access to essential IP,” said Guri Stark, vice president of Marketing, Synopsys Solutions Group. “The addition of Tower’s foundry libraries to the DesignWare Library IP portfolio provides our mutual customers with an even greater array of choices when they need reliable, proven IP.”

Pricing and Availability

The Tower 0.18-micron standard cells, I/Os and memories are currently available for no additional cost to all current DesignWare Library licensees. Tower’s 0.13-micron simulated libraries are expected to be available in the third quarter of this year. Requests to download the Tower libraries can be made at www.synopsys.com/dwrequest.

About DesignWare Library

Synopsys DesignWare IP enables designers to more cost effectively create and verify complex SoCs, ASICs and FPGAs. The broad IP portfolio includes synthesizable implementation IP, hardened PHYs and verification IP. DesignWare IP, combined with Synopsys’ robust IP development methodology, extensive investment in quality and comprehensive worldwide technical support, gives designers a faster, more predictable and lower risk path to chip success. The DesignWare Library portfolio includes foundry libraries, verification IP, AMBA™ bus IP and peripherals, memories, building block IP and microcontrollers. All are available under one license with no additional costs, per use fees, or royalties. For a complete directory of Synopsys IP visit: www.synopsys.com/ipdirectory

About Tower Semiconductor Ltd.

Tower Semiconductor Ltd. is a pure-play independent specialty foundry established in 1993. The company manufactures integrated circuits with geometries ranging from 1.0 to 0.13-microns; it also provides complementary technical services and design support. In addition to digital CMOS process technology, Tower offers advanced non-volatile memory solutions, mixed-signal and

CMOS image-sensor technologies. To provide world-class customer service, the company maintains two manufacturing facilities: Fab 1 has process technologies from 1.0 to 0.35 microns and can produce up to 16,000 150mm wafers per month. Fab 2 offers 0.18-micron and below standard and specialized process technologies, and has a current capacity of up to 15,000 200mm wafers per month. The Tower Web site is located at www.towersemi.com.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA) software for integrated circuit (IC) design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release includes forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, which are subject to risks and uncertainties, including statements regarding (i) the expected benefits and dates of availability of Tower's 0.13-micron process technology transfer, (ii) market demand for 0.18- and 0.13-micron technology manufacturing services, (iii) final qualification of the 0.13 micron process, and (iv) timely and successful validation of 0.13-micron IP offering. These statements are based on Synopsys' and Tower's current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in finalizing the production release of the 0.13-micron technology, uncertainties attendant to any new manufacturing solution and the other factors described in Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2004, in the case of Synopsys, and in Tower's most recent Annual Report on Forms 20-F and 6-K, in the case of Tower, in each case as filed with the Securities and Exchange Commission and the Israel Securities Authority, if applicable.

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